

CIR-S4SUSW2608G (5 fHrBc 1r%)) -)

DDR4 SO-DIMM 2666MHz 8GB

Description	Specifications	
<p>This specification defines the electrical and mechanical requirements for 260 pin, 1.2 V (VDD), Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM SO-DIMM). This DDR4 SO-DIMM is intended for use as main memory when installed in PCs, laptops and other systems.</p> <p>Reference design examples are included which provide an initial basis for DDR4 SO-DIMM designs.</p> <p>Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for DDR4-2666 support. All DDR4 SO-DIMM implementations must use simulations and lab verification to ensure proper timing requirement and signal integrity in the design.</p>	Density	8GB
	Pin Count	260pin
	Type	Unbuffered
	Dimensions	69.60mm x 30.00mm
	ECC	Non-ECC
	Component Config	1G x 8 bit
	Data Rate	2666 MHz
	CAS Latency	19
	Voltage	1.2V
	PCB Layers	8
	Operating Temp.(TCASE)	0°C~+85°C
Module Ranks	Single Rank	

Features

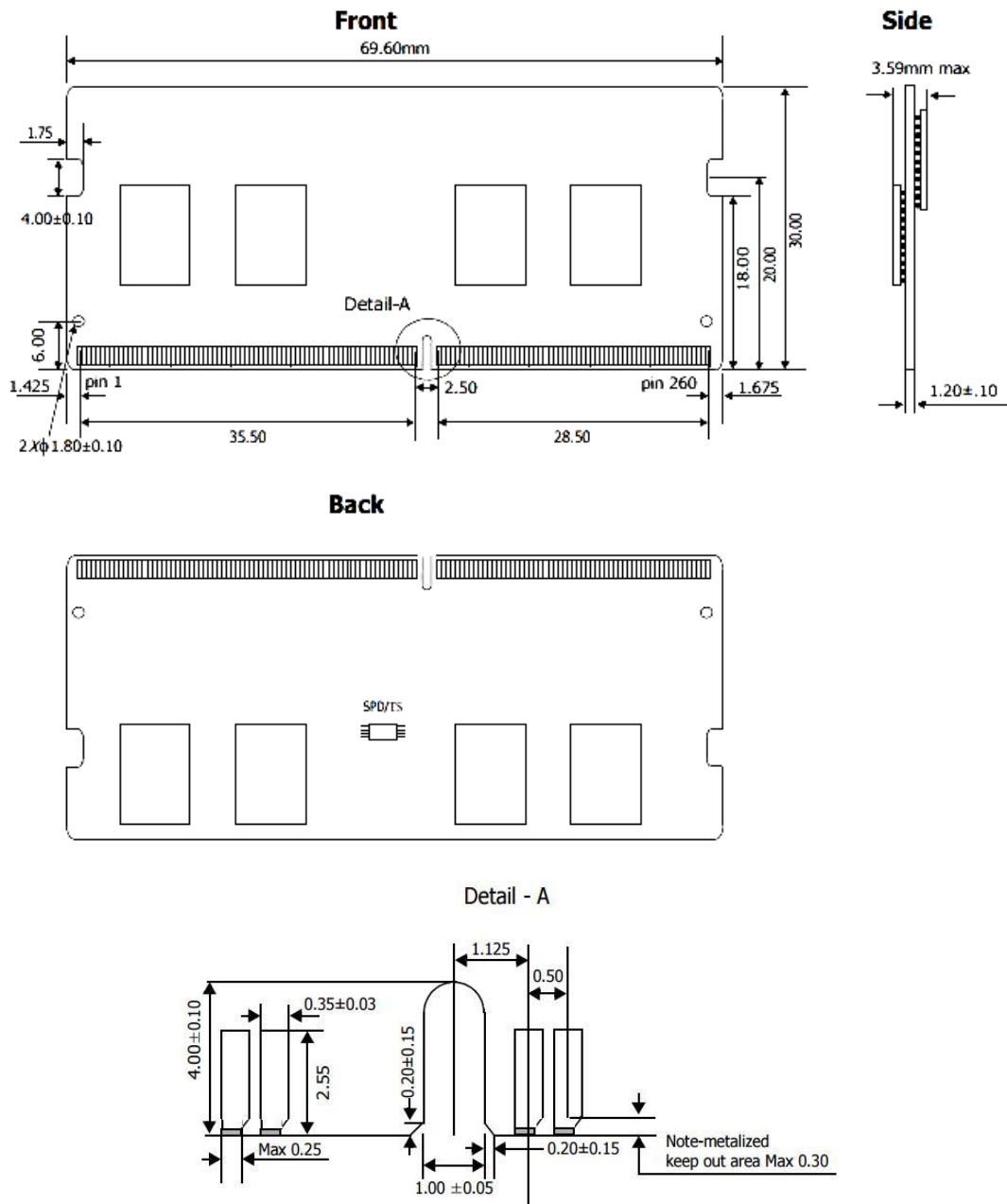
- JEDEC Standard 260-pin Dual In-Line Memory Module
- Intend for PC4-2666 applications
- Inputs and Outputs are SSTL-12 compatible
- VDD=VDDQ = 1.2V±0.06V (1.14V~1.26V)
- Programmable CAS Latency(posted CAS): 11,12,13,14,15,16,17,18,19
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Fly-By topology
- Terminated control, command and address bus
- RoHS and Halogen free

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support								CL-tRCD-tRP
		CL11	CL12	CL13	CL14	CL15	CL16	CL17	CL19	
DDR4-2666	PC4-21300	1600	1600	1866	1866	2133	2133	2400	2666	19-19-19

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified