CIR-W4DUSY2908G Art. no. 162578

DDR4 WIDE TEMP. DIMM 2933MHz 8GB

Description

CIR-W4DUSY2908G is a CMOS Double Data Rate IV (DDR4) Synchronous DRAM module, in Fine Ball Grid Array(FBGA) packages on a 288pin glass-epoxy substrate.

DDR4 unbuffered UDIMM series offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Specifications

Density	8GB
Pin Count	288pin
Type	Unbuffered
Dimensions	133.35mm x 31.25mm
ECC	Non-ECC
Component Config	1G x 8 bit
Data Rate	2933 MHz
CAS Latency	21
Voltage	1.2V
PCB Layers	8
Operating Temp.(TCASE)	-40°C~+85°C
Module Ranks	Single Rank

Features

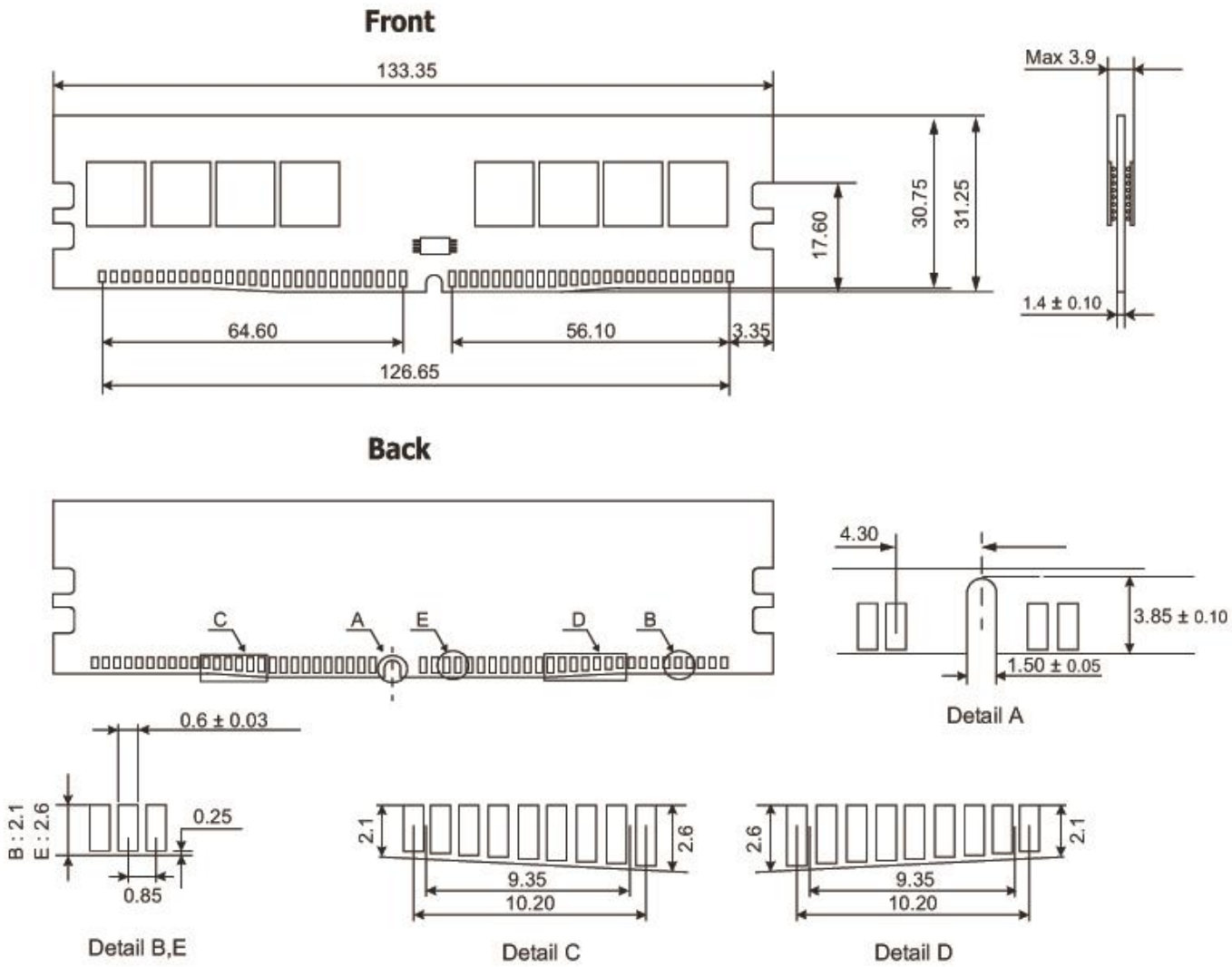
- JEDEC standard
- VDD=VDDQ = 1.2V±0.06V (1.14V~1.26V)
- Inputs and Outputs are SSTL-12compatible
- Programmable CAS Latency(posted CAS): 11,12,13,14,15,16,17,18,19,20,21
- Low-Power auto self-refresh(LPASR)
- SDRAMs have 16internal banks for concurrent operation(4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Fly-By topology
- Terminated control, command and address bus
- RoHS and Halogen free

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support											CL-tRCD-tRP
		CL11	CL12	CL13	CL14	CL15	CL16	CL17	CL18	CL19	CL20	CL21	
DDR4-2933	PC4-23466	1600	1600	1866	1866	2133	2133	2400	2400	2666	2666	2933	21-21-21

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified